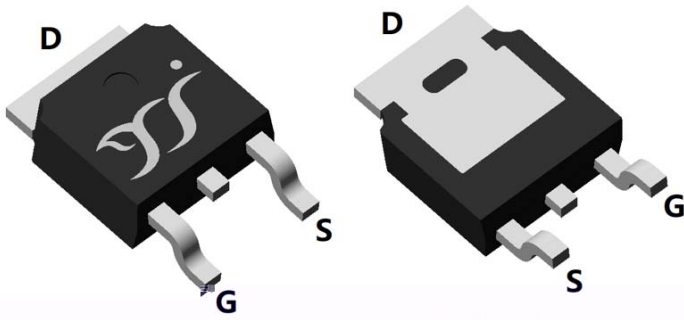


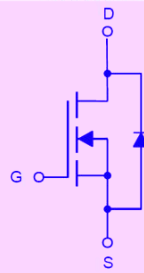
## N-Channel Enhancement Mode Field Effect Transistor



Top View

Bottom View

TO-252



### Product Summary

- $V_{DS}$  100V
- $I_D$  45A
- $R_{DS(ON)}$ ( at  $V_{GS}=10V$ ) 17m $\Omega$
- $R_{DS(ON)}$ ( at  $V_{GS}=4.5V$ ) 21.5m $\Omega$
- 100% UIS Tested
- 100%  $V_{DS}$  Tested

### General Description

- Low  $R_{DS(on)}$  & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- DC-DC convertor

### ■ Absolute Maximum Ratings ( $T_A=25$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	100	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ\text{C}$	$I_D$	7	A
	$T_A=100^\circ\text{C}$		4.5	
	$T_C=25^\circ\text{C}$		45	
	$T_C=100^\circ\text{C}$		28	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	180	A
Avalanche energy <sup>B</sup>		EAS	90	mJ
Total Power Dissipation <sup>C</sup>	$T_A=25^\circ\text{C}$	$P_D$	2.5	W
	$T_A=100^\circ\text{C}$		1	
	$T_C=25^\circ\text{C}$		73	
	$T_C=100^\circ\text{C}$		29	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 +150	$^\circ\text{C}$



## YJD45G10AQ

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient <sup>D</sup>	Steady-State	$R_{\theta JA}$	40	50	°C/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.4	1.7	

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD45G10AQ	F1	YJD45G10A	2500	/	25000	13"Reel



# YJD45G10AQ

## ■ Electrical Characteristics ( $T_J=25$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
		$V_{DS}=100V, V_{GS}=0V, T_J=150^\circ C$	-	-	100	
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=22.5A$	-	14	17	m $\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	17	21.5	
Diode Forward Voltage	$V_{SD}$	$I_S=22.5A, V_{GS}=0V$	-	0.9	1.2	V
Maximum Body-Diode Continuous Current	$I_S$		-	-	45	A
Gate resistance	$R_G$	$f=1MHz, \text{Open drain}$	-	1.4	-	$\Omega$
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V, f=1MHz$	-	1165	-	pF
Output Capacitance	$C_{oss}$		-	265	-	
Reverse Transfer Capacitance	$C_{rss}$		-	8	-	
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=50V, I_D=22.5A$	-	19	-	nC
Gate-Source Charge	$Q_{gs}$		-	6	-	
Gate-Drain Charge	$Q_{gd}$		-	3	-	
Reverse Recovery Charge	$Q_{rr}$	$I_F=22.5A, di/dt=100A/us$	-	45	-	nC
Reverse Recovery Time	$t_{rr}$		-	40	-	ns
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=50V, I_D=22.5A$ $R_{GEN}=2.2\Omega$	-	40	-	ns
Turn-on Rise Time	$t_r$		-	12	-	
Turn-off Delay Time	$t_{D(off)}$		-	55	-	
Turn-off fall Time	$t_f$		-	16	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

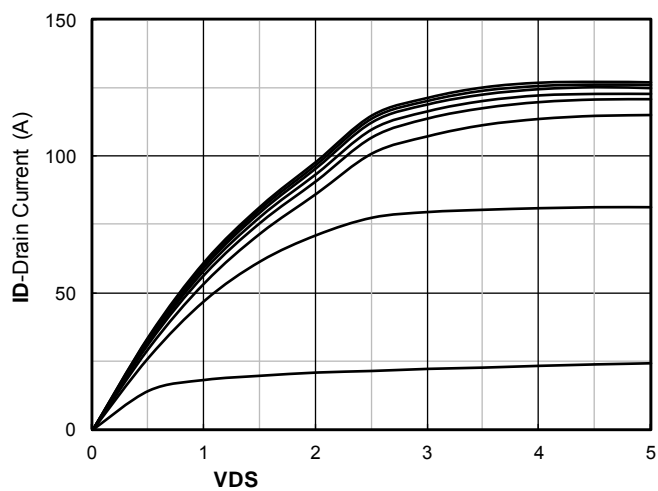
B.  $T_J=25^\circ C, V_{DD}=50V, V_G=10V, R_G=25\Omega, L=0.5mH, I_{AS}=19A$ .

C.  $P_d$  is based on max. junction temperature, using junction-case thermal resistance.

D. The value of  $R_{\theta JA}$  is measured with the device mounted on the minimum recommend pad size, in the still air environment with  $T_A=25^\circ C$ .  
The maximum allowed junction temperature of  $150^\circ C$ . The value in any given application depends on the user's specific board design.



## Typical Electrical and Thermal Characteristics Diagrams





# YJD45G10AQ

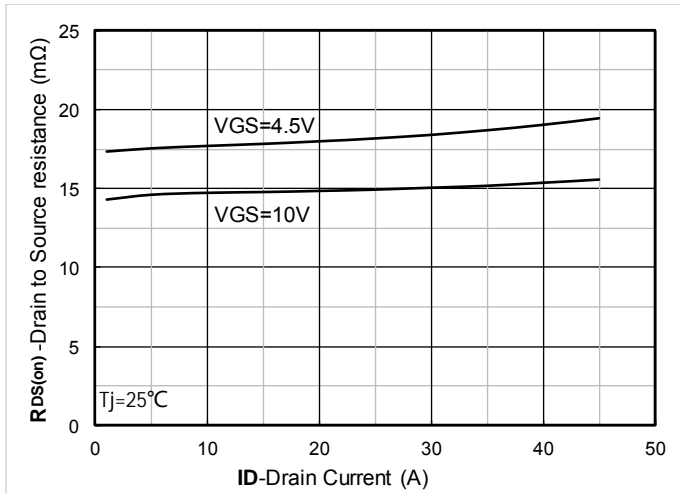


Figure 7.  $R_{DS(on)}$  VS Drain Current

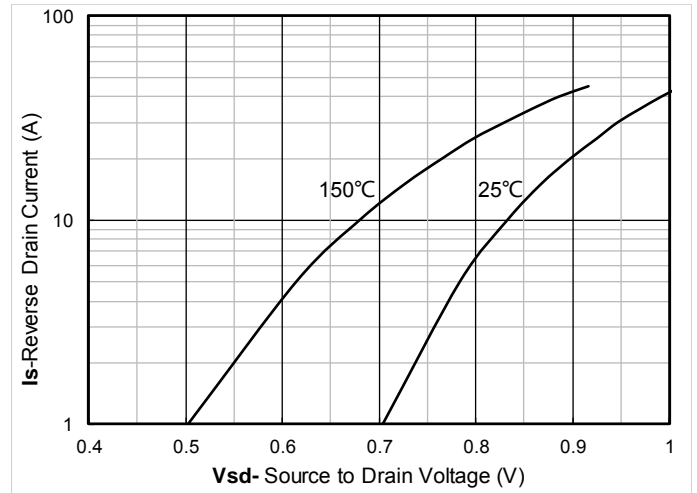


Figure 8.



# YJD45G10AQ

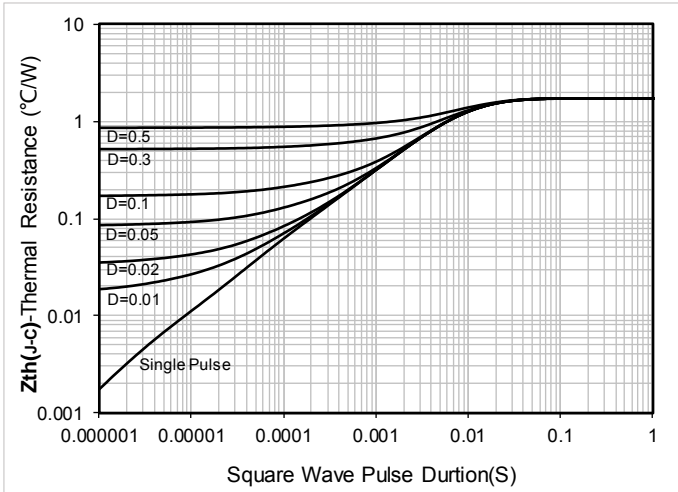


Figure 13. Maximum Transient Thermal Impedance

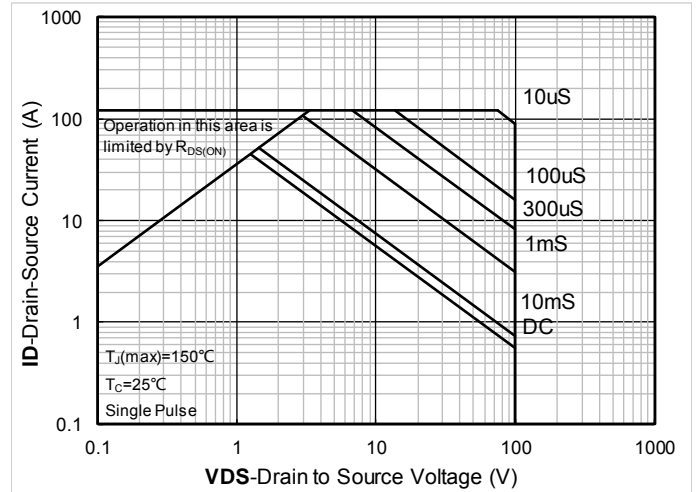


Figure 14. Safe Operation Area

## ■ Test Circuits & Waveforms

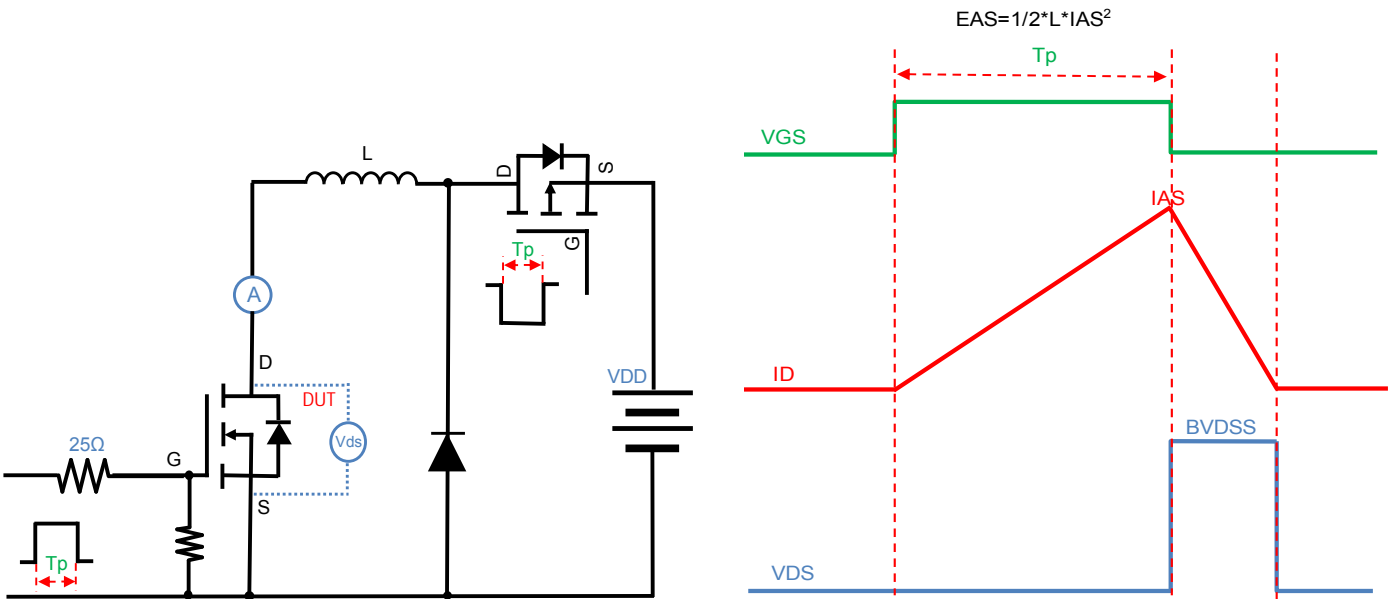


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

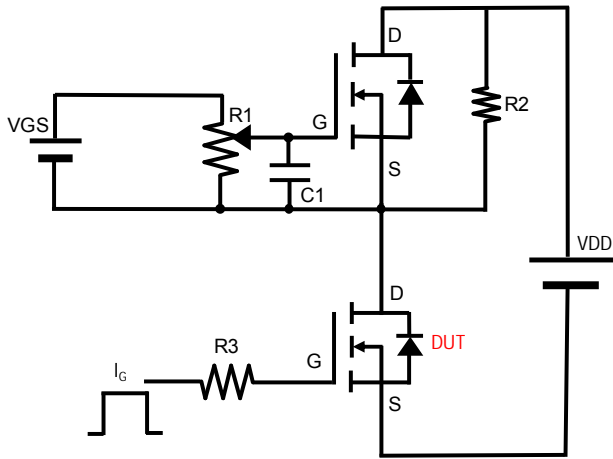


Figure B. Gate Charge Test Circuit & Waveform

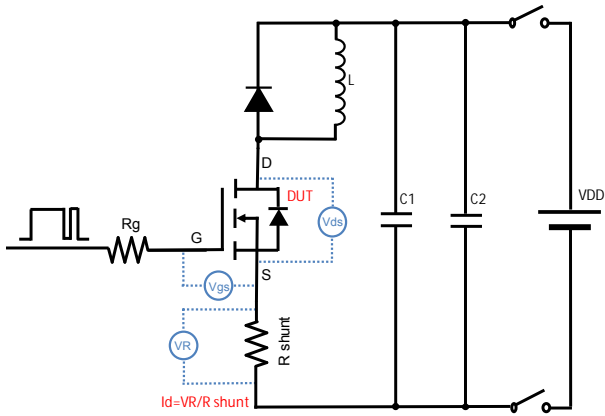


Figure C. Resistive Switching Test Circuit & Waveform

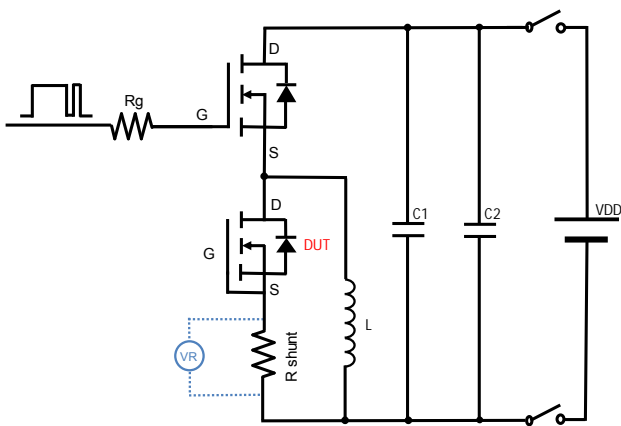
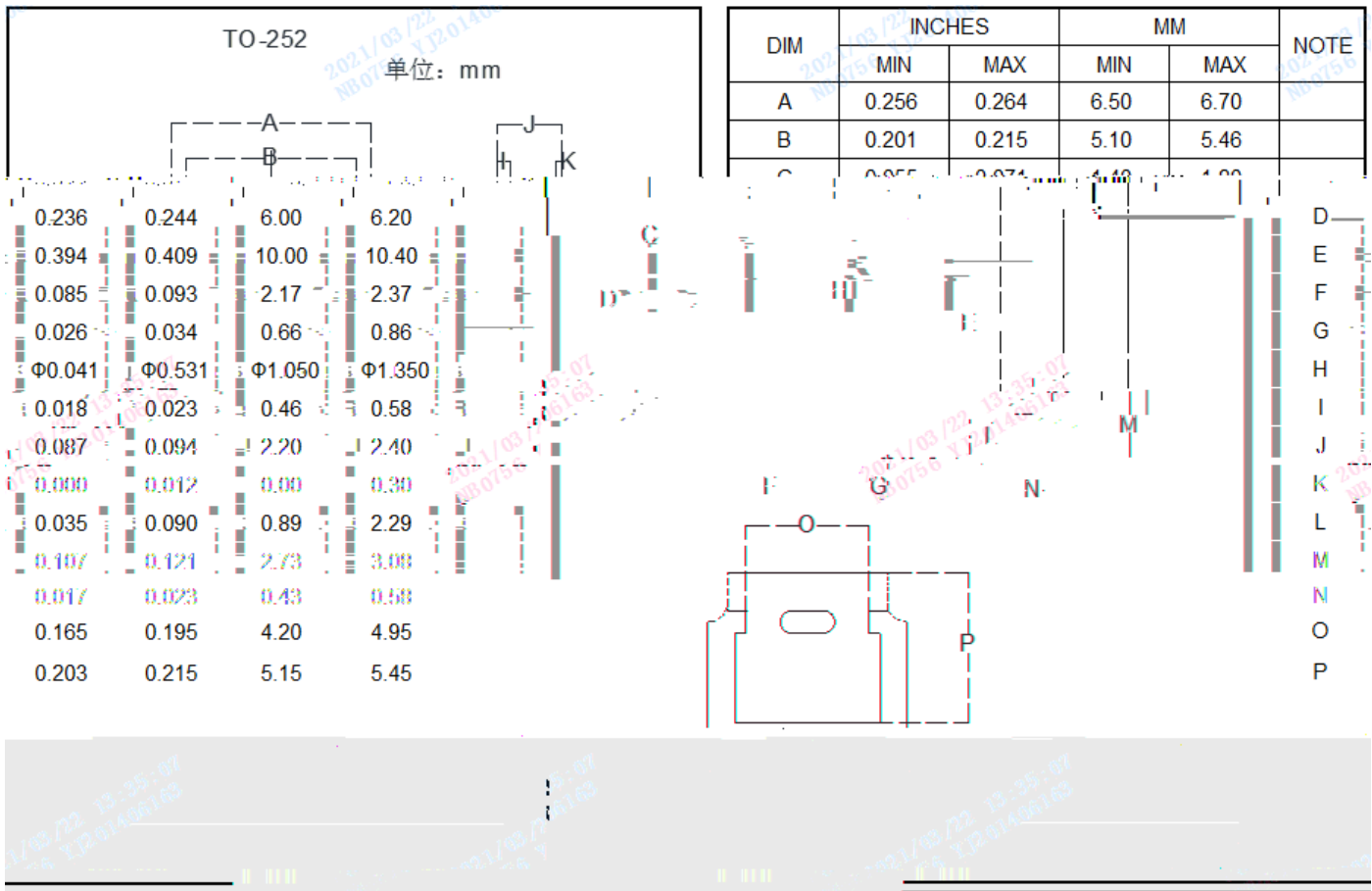


Figure D. Diode Recovery Test Circuit & Waveform

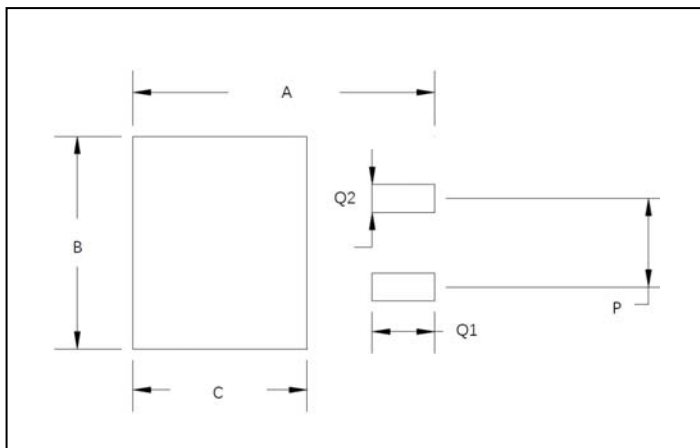


# YJD45G10AQ

## TO-252 Package information



## Suggested Pad Layout



Dim	Millimeters
A	11.4
B	6.74
C	6.23
P	4.56
Q1	2.28
Q2	1.52