







Schematic



Pin Configuration
1. Anode
2. Cathode
3. Emitter
4. Collector

-10

4-

	( 2		
		60	
		125	
		6	
		100	
		0	
		7	
		50	
		150	
•		250	
*1		5000	
		-55 + 110	
		-55 + 125	1
*2		260	1

\*1 , . . 40 60% . . 1

3, 4

\* 2 10

> 2 201

1, 2



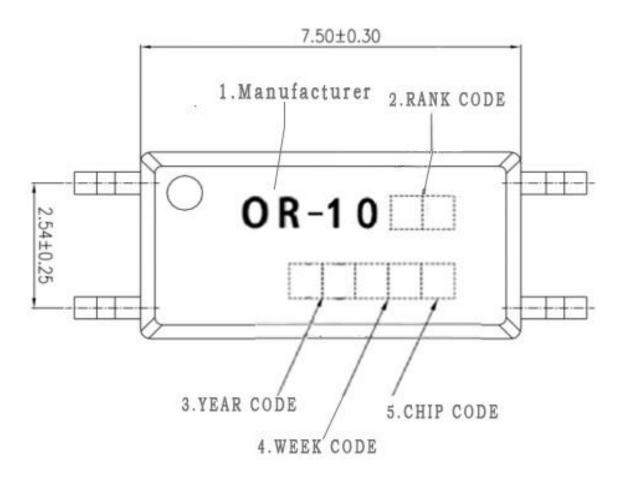
		50		1.25	1.6	
		4			10	
		0, 1		50		
		20 , 0		10	100	
		1 0	0			
		0.1	7			
		5	50		600	%
		5	2.5		30	
	( )	10 1			0.3	
		500 40 60%	10 <sup>12</sup>			
		0, 1	1	0.3		
		5,		3	1	
		100		4.7	1	

-10

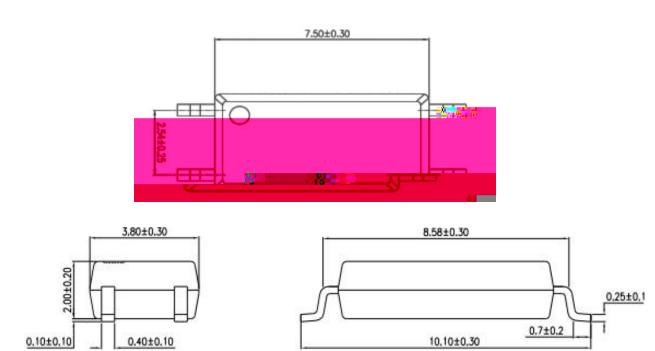


² Ws^•BWYr)Uā y2ñ0 R•U"s€•1Q5 R•^ " 0 Ÿ P XS!0 @

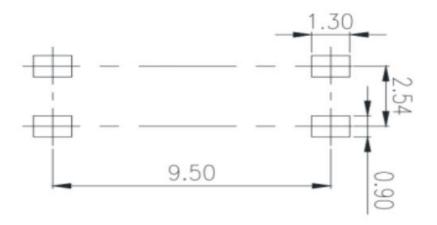




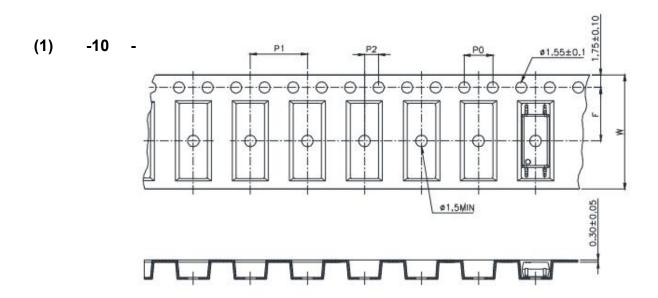


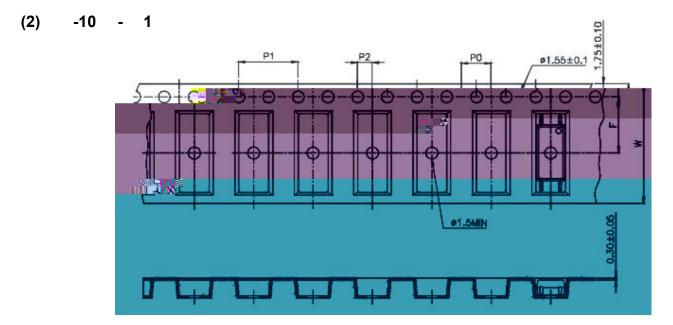


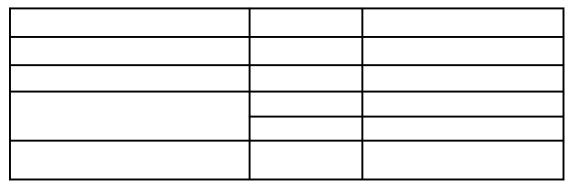








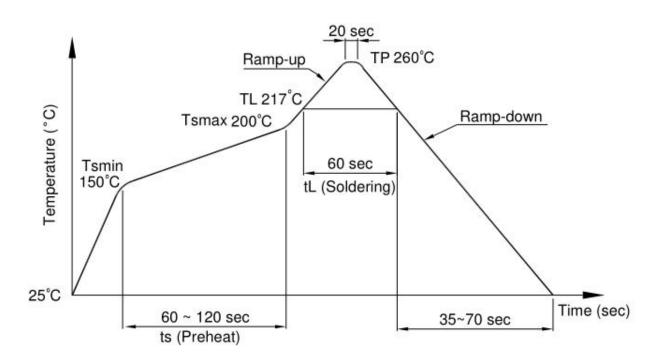






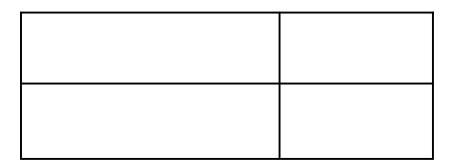


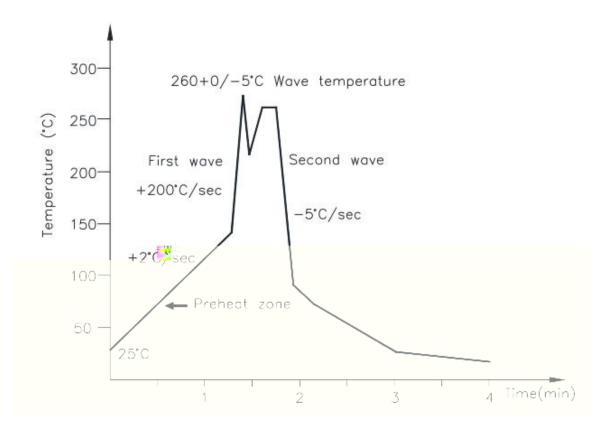
(1). ( - -020 )



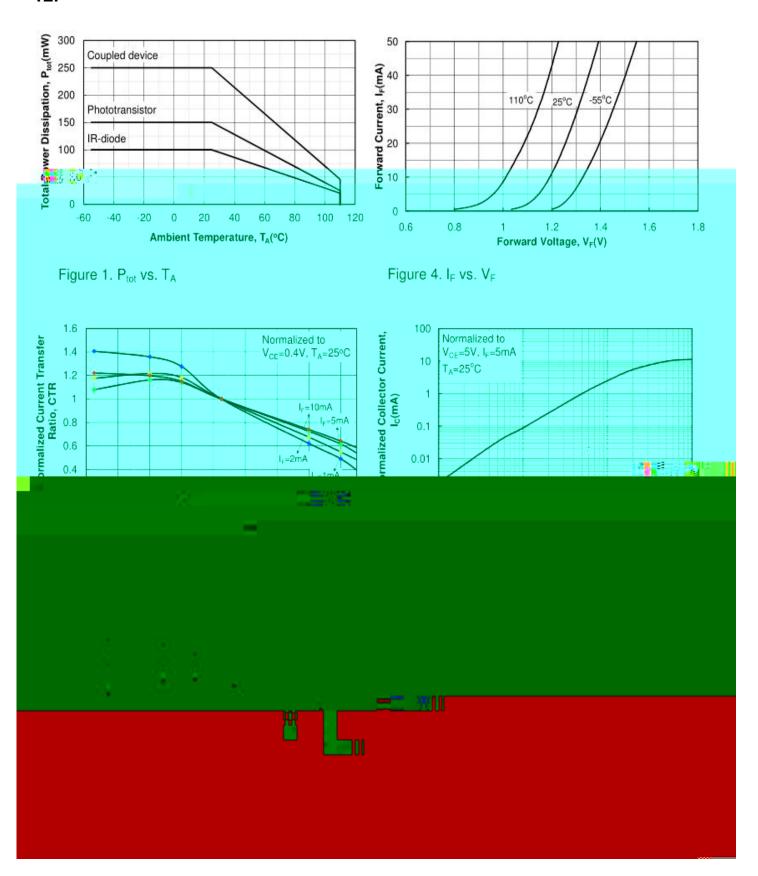


(2). ( 22 111 )

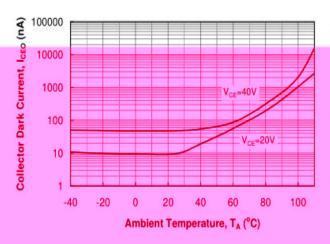












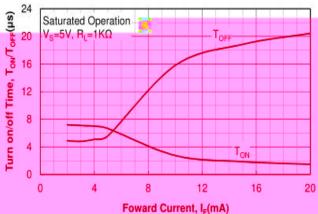
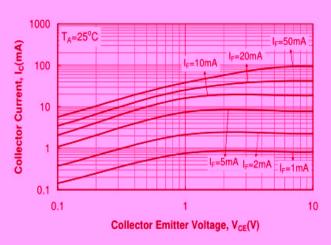


Figure 7. I<sub>CEO</sub> vs. T<sub>A</sub>

Figure 10.  $T_{ON} / T_{OFF} vs. I_F$ 



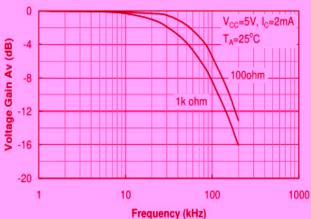


Figure 8. I<sub>C</sub> vs. V<sub>CE</sub>

Figure 11. Frequency Response



Figure 9 Fig

